

ABSTRACT OF THE DISCLOSURE

In a variable-gain digital filter of the prior art in which  $X$  is the number of bits of data after baseband processing and  $Y$  is the number of gain bits, the number of 5 bits of input is  $X + Y$  and the number of flip-flops required is equivalent for  $(X + Y) \times n$  bits, thereby raising the problem of excessive circuit scale. In the variable-gain digital filter of the present invention, a selector and multiplier for regulating gain are arranged 10 inside the digital filter whereby the number of bits of filter input is  $X$ , the number of flip-flops inside the filter is  $X \times n$  bits, and a  $(Y \times n$  bit) reduction in the number of flip-flops is enabled. The gain regulation circuit that was arranged to precede the prior-art filter 15 is thus incorporated within the digital filter to enable a reduction in circuit scale.